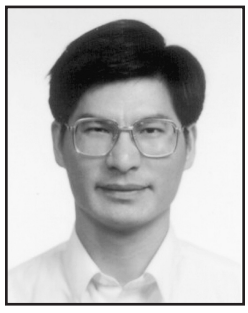
Session 15 Overview

Multimedia and Parrallel Signal Processors



Chair: Michel Harrand, *CEA/LIST, Gif-sur-Yvette, France*

Associate Chair: Liang-Gee Chen, *National Taiwan University, Taipei, Taiwan*

Consumer electronics equipment such as game consoles, mobile handsets, home entertainment, or automotive security systems have become a major driver for high-performance yet low-power signal processing circuits. The diversity of new emergent standards adds a requirement for flexibility as an increasingly important feature of these systems. The trade-off between flexibility, performance and power consumption is addressed through a wide range of architectures mixing programmable and dedicated blocks.

On one extremity of this scale are massively parallel processing systems for applications such as video scene analysis like those presented in the first half of this session. On the other side of this scale are dedicated circuits for 3D graphics or video encoding/decoding still supporting several standards and offering programmable trade-offs between performance and power consumption. Examples of such circuits are presented in the second part of the session.

The first two papers present completely different massively parallel processing architectures:
Paper 15.1 from Philips and NXP presents a single-instruction multiple-data (SIMD) processor well-suited to the frame-iterative algorithms required by video scene analysis applications. It features 320 processing elements providing 107GOPS for a power consumption of 600mW, and 10M on-chip memory able to store up to 4 VGA images interconnected through a 1.3Tb/s network. An innovative internal feedback path is provided to have a low-cost look-up table for the vector data.

Paper 15.2 from Stream Processors and Stanford presents a stream processor based on a VLIW architecture. The chip features 80 parallel ALUs organized into 16 data-parallel lanes running at 800MHz, and 2 CPU cores. It provides 512 8b GOPS at a power consumption of 0.082mW/MMAC (16b).

Paper 15.3 from Renesas, NTT DoCoMo, Fujitsu, Mitsubishi and Sharp presents a chip integrating a dual-mode WCDMA-HSDPA/GSM-EDGE baseband with multimedia functions such as MPEG4 and H.264 video codecs, 3D graphics, and GPS. It includes 3 processor cores running up to 390MHz and dedicated hardware accelerators. In order to optimize static power consumption, the chip is split into 23 power islands, and a retention mode is implemented on its cache memories. Dynamic power consumption reduction is addressed through a dynamic bus-clock stop scheme. Bandwidth with the external SDRAM is minimized through a specific on-chip interconnection buffer.

The next two papers in this session demonstrate novel designs for 3D graphics processing:
Paper 15.4 from KAIST presents a 36 frames/s SXGA 3D display processor with a programmable 3D graphics rendering engine. This is the first implementation of a real-time 3D display processor. The integrated rendering engine supports Pixel Shader 3.0 and OpenGL ES 2.0, which supports advanced functionalities that provides users with a realistic experience in real-time interactive 3D applications like games and GUI.

Paper 15.5 from KAIST presents a 52.4mW 3D graphics processor with 141Mvertices/s vertex shader and 3 power domains of dynamic voltage and frequency scaling. This graphic processor is 17.5% faster, consumes 50.5% less power and takes 35.4% less area than previous designs. It presents the first unification of floating-point vector, transcendental and matrix operations in a single arithmetic platform. The chip also improves its power efficiency by using 3 power domains of dynamic voltage and frequency scaling.

Paper 15.6 from National Chung-Cheng U and National Yun-Lin UST presents the first dynamic quality-scalable H.264 video encoder chip suitable for power-adaptive video applications. With 0.13µm CMOS technology, the chip consumes 7mW~183mW in encoding CIF~HD720 videos at the cost of 470kgates and 13.3kB SRAM. Compared to the state-of-the-art design for real-time HD720 video encoding, it presents a reduction of 49% in gate count and 61% in internal memory.

The final paper, Paper 15.7 in this session from National Chung-Cheng U and Feng-Chia U introduces a 71mW 252kgates Multi-Standard Multi-Channel Video Decoder for High Definition Video Applications. This design provides decoding functionalities for JPEG/MPEG-1/2/4/H.264 image/video standards. Through a 70% reduction in external memory bandwidth and 60% reduction in computational complexity, the proposed chip reduces gate count by 72% and power consumption by 87% as compared to the state-of-the-art design in 0.13µm CMOS technology.

15.1 XETAL-II: A 107GOPS, 600mW Massively-Parallel Processor for Video Scene Analysis **1:30 PM**

A. Abbo, Philips Research, Eindhoven, The Netherlands

Xetal-II is a SIMD processor with 320 processing elements delivering a peak performance of 107GOPS on 16b data while dissipating 600mW. A 10Mb on-chip memory can store up to 4 VGA frames allowing efficient implementation of frame-iterative algorithms. A massively parallel interconnect provides an internal bandwidth of more than 1.3Tb/s to sustain the peak-performance. The 74mm^2 IC is fabricated in 90nm CMOS.

15.2 A Programmable 512GOPS Stream Processor for Signal, Image, and Video Processing **2:00 PM**

B. Khailany, Stream Processors, Sunnyvale, CA

A 34M transistor stream processor SoC for signal, image, and video processing contains 80 parallel integer ALUs organized into 16 data-parallel lanes with a 5-ALU VLIW per lane, two CPU cores and I/Os. Implemented in a 0.13µm CMOS technology, sixteen 800MHz data-parallel lanes combine to deliver performance of 512 8b GOPS or 256 16b GOPS.

15.3 A 390MHz Single-Chip Application and Dual-Mode Baseband Processor in 90nm Triple-V_t CMOS **2:30 PM**

M. Ito, Renesas Technology, Tokyo, Japan

A single-chip 11.15×11.15mm^2 application and dual-mode WCDMA/HSDPA and GSM/EDGE baseband processor achieves 390MHz in triple-V_t low-power 90nm 8M CMOS. A CPU core standby mode with resume cache reduces leakage current of each CPU to 0.04mA when idle. A dynamic bus clock-stop scheme further reduces power consumption. Interconnect buffers allow the chip to support 30f/s VGA video.

15.4 A 36fps SXGA 3D Display Processor with a Programmable 3D Graphics Rendering Engine **3:15 PM**

S-H. Kim, KAIST, Daejeon, Korea

A 3D display processor with a programmable 3D graphics rendering engine is implemented. The integrated rendering engine supports Pixel Shader 3.0 and OpenGL ES 2.0. A 3D image synthesis engine generates 3D images at 36fps. The die contains 1.74M gates and occupies 5×5mm^2 in 0.18µm CMOS and dissipates 379mW at 1.8V.

15.5 A 52.4mW 3D Graphics Processor with 141Mvertices/s Vertex Shader and 3 Power Domains of Dynamic Voltage and Frequency Scaling **3:45 PM**

B-G. Nam, KAIST, Daejeon, Korea

A 3D graphics processor fabricated using 0.18µm 6M CMOS contains 1.57M transistors and 29kB SRAM in a core size of 17.2mm^2. The vertex shader utilizes a logarithmic number system for 141Mvertices/s and the 3 power domains are controlled separately by dynamic voltage and frequency scaling for 52.4mW at 60fps.

15.6 A 7-to-183mW Dynamic Quality-Scalable H.264 Video Encoder Chip **4:15 PM**

H-C. Chang, National Chung-Cheng University, Chia-Yi, Taiwan

A dynamic quality-scalable H.264 video encoder is presented for power-adaptive video encoding. In 0.13µm CMOS technology, it requires 470kgates/13.3kB SRAM and consumes 7mW/183mW in encoding 30fps CIF/HD720 video. Compared to the state-of-the-art design for real-time HD720 video encoding, a 49% reduction in gate count and a 61% reduction in internal memory is achieved.

15.7 A 252kgate/71mW Multi-Standard Multi-Channel Video Decoder for High-Definition Video Applications **4:45 PM**

C-D. Chien, National Chung-Cheng University, Chia-Yi, Taiwan

A multi-standard (JPEG/MPEG-1/2/4/H.264) video decoder includes 252kgates and 4.9kB internal memory in a core size of 4.2×1.2mm^2 using 0.13µm 1P8M CMOS. The power consumption at 1.2V supply is 71mW at 120MHz for real-time HD1080 and 7.9mW at 20MHz for real-time H.264 decoding of D1 video.